

## **What's New in Cadence OrCAD 16.2 Release**

The new OrCAD release 16.2 boasts a sweeping set of improvements aimed at increasing performance and productivity through new features and functionality. The new technology helps deliver shorter, more predictable design cycles for PCB designs. The OrCAD 16.0 release made a significant investment in improving the ease of use of Cadence OrCAD PCB Editor. The new release continues this emphasis on improving ease of use for all products in OrCAD PCB design technologies, from design creation tools in the front end to PCB layout tools in the back-end.

### **Cadence OrCAD Capture**

Cadence OrCAD Capture boasts productivity and usability improvements including an updated GUI, enhanced search capabilities and new capability for designing-in FPGAs.

- Usability Enhancements - In OrCAD release 16.2, OrCAD Capture and Cadence OrCAD Capture CIS come with many enhancements to provide an improved usability experience to users. Starting from new ways of managing multiple windows to the ability to place wires and parts using a crosshair cursor; all enhancements are created to increase ease of use.
- Enhanced OrCAD Capture and OrCAD PCB Editor Integration - OrCAD Capture 16.2 comes with better integration with OrCAD PCB Editor. The cross probing and cross placement features enhance flow between OrCAD Capture and OrCAD PCB Editor.
- OrCAD Capture FPGA Design-in - New FPGA design-in features include the ability to create split symbols, import and export FPGA pin assignments for leading FPGA vendors tools, and ease-of-use improvements for supporting the ECO process for FPGAs.
- New Annotation Type Option - The annotation dialog box now includes a new annotation type list. When annotating your design you can now choose from three sequence options: Default, Left – Right, and Top – Bottom.
- DRC Enhancements - The design rules check in OrCAD Capture is enhanced to improve performance on very large designs and to include some new design checks.
- Netlist Enhancements - OrCAD Capture release 16.2 includes a new PACK\_SHORT property used to short pins on a part. Multiple groups of pins, each group having two or more pins, can be shorted. Users no longer need to update invisible pins because the correct net names are updated for invisible power pins if there is a global net short and a POWER\_GROUP is not specified.
- OrCAD Layout to OrCAD PCB Editor - The OrCAD Layout to OrCAD PCB Editor Translator has been enhanced for converting PCB designs created in OrCAD Layout to OrCAD PCB Editor.
- OrCAD PCB Editor integration in OrCAD Capture - OrCAD Capture now provides an automatic sync-up of the original schematic design with the translated board design.
- User Interface Updates - In OrCAD 16.2, OrCAD Capture and OrCAD Capture CIS have been upgraded with a new, softer look. This upgrade brings uniformity across many of the generic styles in different Cadence products. All new icons have also been added across the functional groups.

## **Cadence OrCAD Capture CIS**

OrCAD Capture CIS release 16.2 features Relational Data Management Support that allows users to create and use relational tables in the CIS parts database. This new release also contains all of the productivity and usability improvements highlighted in OrCAD Capture.

- Relational Database Management Support - With 16.2, OrCAD Capture CIS allows you to create and use relational tables in your parts database. These tables must have a one-to-many relationship with your part information tables. The database may contain a vendor table with multiple manufacturer part numbers for one company part number in your electrical table. This structure allows you to query for data across the primary and relational tables.
- OrCAD Capture CIS Configuration File in XML Format – The OrCAD Capture CIS configuration file is in XML format. Giving you the flexibility to read and edit in any text or XML editor.
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- Usability Enhancements - In OrCAD release 16.2, OrCAD Capture and OrCAD Capture CIS come with many enhancements to provide an improved usability experience to users. Starting from new ways of managing multiple windows to the ability to place wires and parts using a crosshair cursor; all enhancements are created to increase ease of use.

## **Cadence PSpice A/D**

Cadence PSpice® A/D release 16.2 continues to provide user with robust and predictive simulation technology. The new release presents productivity and usability improvements including an updated GUI, new models and modeling support, and CheckPoint Restart for digital and mixed signal circuits.

- New MOSFET Device Model BSIM4 Support - BSIM4 provides robust and predictive simulations with increased accuracies in modeling various functions, such as tunneling and thermal noise. With BSIM4 support, PSpice A/D now integrates the following models: IV model, GIDL (gate-induced drain leakage) Current model, Bias-Dependent Source/Drain Resistance (Rds(V)) model and Asymmetric Source/Drain Junction Diode model
- Enhanced Performance for Large DAT Files - PSpice A/D takes much lesser time to load large DAT files that are more than 2 GB in size. In addition, the percentage progress of loading is displayed on the status bar, making it easier for users to approximate the load time.
- New Vendor Models – The following vendor models have been added to PSpice A/D: 8-bit Shift Register CD4094BC, ABM for Digital Primitive, ARINC-429 Drivers, Dual High Side MOSFET Driver, Gate Turn Off Thyristor (GTO), LOGIC Gate OptoCouplers, Low Dropout Adjustable Regulator LM2941, Microsemi Bidirectional suppressor, On-Semi Microprocessor supervisor circuit, Planar Core Models, Precision Isolation Amplifier, Precision Voltage Reference, SAC Models and Surface Mount Zener Voltage Regulator
- Check-Point restart for mixed-signal designs - The CheckPoint Restart feature can be used to generate CheckPoints at specified time-points within a simulation. In PSpice A/D release 16.2, this feature is now available for digital and mixed circuits. Engineers are able to restart and run simulations from a range of interest instead of running the simulation again from start for any changes
- User Interface Updates - In PSpice A/D and Cadence PSpice Advanced Analysis have been upgraded with a new, softer look. This upgrade brings uniformity across many of the

generic styles in different Cadence products. All new icons have also been added across the functional groups.

## **Cadence PSpice Advanced Analysis**

PSpice Advanced Analysis release 16.2 has enhanced Smoke Analysis with additional device support. This new release also contains all of the productivity and usability improvements highlighted in PSpice A/D.

- New Supported Devices in Smoke Analysis – Inductor for DC Current, \_ Inductor for DC Current, VSWITCH, Transformer (Single and Double Winding) and Electrolytic Capacitor. In addition, now you can add Smoke parameters to the following new devices in the PSpice Model Editor: LED, Zener Diode, Varistor, Diode Bridge, GaAs MESFET, Thyristor, Voltage-Controlled Switch, 4 Pin Optocoupler, NPN-PNP, NMOS-PMOS, Dual BJT, Dual MOS and Transformer
- User Interface Updates - In PSpice A/D and PSpice Advanced Analysis have been upgraded with a new, softer look. This upgrade brings uniformity across many of the generic styles in different Cadence products. All new icons have also been added across the functional groups.

## **Cadence OrCAD PCB Editor**

Cadence continues the major development effort in the area of usability in the OrCAD PCB Editor. The 16.2 release focuses on productivity improvements in etch edit and component placement, color and graphics, and manufacturing applications.

- Same Net Spacing Rules - in 16.2 same net spacing rules are now managed entirely within the new Same Net Spacing domain in Constraint Manager. The new domain provides robust capability required for same net rules. Each Spacing DRC in the system now has a respective Same Net DRC. Same Net DRC values can now be set independently of Net to Net Spacing DRCs.
- Via-in-Pad DRC - A new suite of DRC checks ensures the placement of vias is properly contained within SMD pads. Via-in-Pad checks are run at the design level but override capability at the symbol level is possible with properties.
- Tangent Rule Adherence - As a result of etch edit alignment with the Same Net DRC system, the sliding of vias to be tangent with other vias or pins is now done effortlessly.
- Sliding Via-in Pad - Sliding a via located in a pad to a point outside the pad boundary now produces a cline attachment. Prior to 16.2 this resulted in an orphan via.
- Dynamic Unused Pad Suppression - The Unused Pad Suppression User Interface controls the suppression state for pins and/or vias. Suppression can be applied to any or all of the inner signal subclasses. Exceptions include Top/Bottom layers, Negative Planes and Begin/End layers of B/B vias.
- Exception Properties – New in 16.2, Exception Properties prevent pads from being removed at the symbol, net, pin and via level. They also can be used to allow pad removal on outer layer elements.
- New Suite of Drill-Based DRCs - A new class of Hole-based checks, supported in both Spacing and Same Net Domains of Constraint Manager, provides the DRC capability when Unused Pad Suppression is enabled or pad definitions are set to null. A Hole to Metal check is performed only when the respective hole is void of pads on conducting layers. When pads are present, the hole check yields to the convention pin and via checks.

- User Definable Mask Layers - The padstack definition now supports a maximum of 16 user-definable mask layers. Mask layers can be used for HDI via plugging, filling, capping or other masking applications like silver and hard and soft gold.
- Non-Standard Drill Types - Additional HDI drill types are available in the Non-standard Drill section of the Padstack Editor. Use non-standard attributes to control NC Drill output.
- Slotted Vias - Plural vias are used in high-current applications. The Multiple Drill section of the Padstack Editor form now supports negative clearance entries for slot formation.
- Etch Turn Under SMD Pin - This check is designed to detect etch compensation buried within the pad. Driven by concern that etch segments within pad boundaries adversely affect timing rules, the checker reports if more than two vertex point is located within the pad boundary.
- Mechanical Pin to Metal - Mechanical pins are non-logical elements, typically used as mounting or tooling holes and fiducials. Manually drawn keep-out areas are traditionally attached to the mechanical symbol to restrict etch around the perimeter of the hole or pad. A new pad usage option, Enable Anti-pads as Route Keep-outs (ARK), permits the anti-pad associated with the padstack of the mechanical pin to be used as an implicit route keep-out area. The mechanical pin checks are located in the Design Modes form.
- Snap Integration Across Edit Commands - Snapping functionality has been integrated to many editing commands associated with backend SPB products. Applications involving the use of snap may include the manual placement of mechanically constrained components such as connectors, key pads, or mounting holes to targets imported from an MCAD system or snapping a testvia to a fixture probe location. There are 11 snap options available on the right-mouse-button menu of most editing commands (move, slide, and place manual), for example.
- Usability Enhancements - In OrCAD release 16.2, OrCAD PCB Editor comes with many enhancements to provide an improved usability experience to users.